

## **REMARKS**

The Office Action dated September 30, 2005, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-15 are currently pending and are respectfully submitted for consideration.

Claims 1-15 were again rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,625,146 of Merchant et al. ("Merchant") in view of U.S. Patent No. 6,625,146 of Denio et al. ("Denio"). The Office Action states that Merchant teaches all of the elements of claims except "a fast filtering processor filtering the data coming into one data port interface and taking selective filtering action based upon a filtering result," "fast filtering processor being programmable by the CPU," "a fast filtering processor applying a filtering mask to a packet, providing a filter result, applying the filter result to predetermined rules in the indexed rules table, and flows of data are updated based upon the filtering," "the fast filter processor including a set of exclusive filter masks and inclusive filter masks, where the exclusive filter masks are configured to exclude all packets with which there is a match with the filter results," "filter masks which filter ingress and egress port fields and filter select fields of an incoming packet," and "the fast filtering processor for filtering incoming packets in order to determine what specific actions should be taken to further modify the packet handling." The Office Action supplies Denio to remedy these deficiencies. Applicants respectfully traverse this rejection.

Claim 1 is directed to a network switch for network communications. The network switch includes a first data port interface supporting a plurality of data ports transmitting and receiving data at a first data rate, a second data port interface supporting a plurality of data ports transmitting and receiving data at a second data rate, a CPU interface configured to communicate with a CPU, an internal memory communicating with the first data port interface and the second data port interface, a memory management unit including an external memory interface for communicating data from at least one of the first data port interface and the second data port interface and an external memory and a communication channel communicating data and messaging information between the first data port interface, the second data port interface, the CPU interface, the internal memory, and the memory management unit. One data port interface of the first data port interface and the second data port interface includes a fast filtering processor filtering the data coming into the one data port interface and taking selective filter action based upon a filtering result. The one data port interface further includes a flow monitor for monitoring flows of data through the network switch, where a flow of the flows of data is defined by a combination of a source address and a destination address for a portion of the data passing through the network switch. Claims 2-9 depend from claim 1.

Claim 10 is directed to a method of handling data packets in a network switch. The method includes the steps of placing incoming packets into an input queue, applying the input data packets to an address resolution logic engine, performing a lookup to determine whether certain packet fields are stored in a lookup table and determining

index values for the input data packets, filtering the incoming packet through a fast filtering processor in order to determine what specific actions should be taken to modify the packet for further handling and discarding, forwarding, or modifying the packet based upon the filtering. The index values are used by the fast filtering processor to rapidly find an indexed specific action of the specific actions. Claims 11 and 12 depend from claim 10.

Claims 13 is directed to a network switch for handling data packets including means for placing incoming packets into an input queue, means for applying the input data packets to an address resolution logic engine, means performing a lookup to determine whether certain packet fields are stored in a lookup table and means for determining index values for the input data packets, means for filtering the incoming packet through a fast filtering processor in order to determine what specific actions should be taken to modify the packet for further handling and means for discarding, forwarding, or modifying the packet based upon the filtering. The index values are used by the fast filtering processor to rapidly find an indexed specific action of the specific actions.

As discussed in the present specification, the present invention enables the filtering of packets based on packet flows. It is respectfully submitted that the cited art of Merchant and Denio fails to disclose or suggest the elements of any of the above-discussed claims. Therefore, the prior art fails to provide the critical and unobvious advantages discussed above.

Merchant is directed to a method and apparatus for operating a network switch in a CPU-less environment. The switch is designed to receive an initialization signal and an internal rules checker begins to process data frames based on source and destination addresses. The Office Action correctly notes that Merchant fails to disclose a fast filtering processor filtering data coming into one data port interface and taking selective filter action based upon a filtering result.

Denio is directed to a switch that reduces broadcast traffic in a network. The Office Action alleges that the forwarding module of Denio is equivalent to the fast filtering processor claimed. However, the forwarding module “that allows the switching device 200 to filter out all broadcast traffic for specified ports.” (Column 4, lines 63-65). Thus, filtering is only performed when a packet is destined for specified ports, as opposed to based on specific fields in the packet, as discussed and claimed in the instant invention.

Claim 1 recites, in part, “a flow monitor for monitoring flows of data through the network switch, where a flow of the flows of data is defined by a combination of a source address and a destination address for a portion of the data passing through the network switch.” Both Merchant and Denio are silent with respect to the use of flows, where the definition of flows is recited in claim 1.

The concept of flows is missing from both Merchant and Denio. In the Response to Arguments section, the Office Action asserts that a flow monitor, broadly construed, is taught by Merchant’s element 40. Applicants respectfully disagree. Merchant’s element 40 is an internal rules checker (IRC). As Merchant explains, the IRC contains an IRC

controller 82, an address table 84, and a sending address lookup logic 90. Merchant's IRC is described as supporting (with its address table) 4096 user addresses and 64 VLANs. The IRC is used to keep broadcast traffic "inside" a particular VLAN. The IRC does a source address and destination address search, not to determine a flow, but rather to make a frame forwarding decision.

As col. 12, ll. 1-31 of Merchant explains, first the IRC controller searches the bin list for an address entry whose address, VLAN index, and receive port number fields match the source address, VLAN index, and receiver port of the received frame. If a match is found, the controller sets the hit bit for that address entry, and then searches the address table for an entry that includes the destination address and VLAN index of the frame. If a match is found, the IRC controller uses the port vector field of the address entry to generate the forwarding descriptor. If there is no match for the destination address and VLAN index, the frame is flooded to all members of the VLAN. As explained in the specification and as defined in claim 1, a flow is defined as a plurality of packets that have the same source and destination address. Merchant and Denio do not discuss flows nor do they monitor flows.

For example, there is no indication that Merchant checks the destination address unless the source address, VLAN index, and receive port number all match an entry in the bin list. This is because Merchant is not interested in monitoring flows defined as packets having the same source and destination address, but only in identifying frames

with characteristics that require them to be forwarded singly or flooded forward. In short, Merchant does not disclose or suggest a flow monitor.

Additionally, Applicants note that the Office Action does not establish that Merchant's IRC is part of one of at least two data port interfaces, as recited in the claim. Accordingly, Applicants submit that the Office Action does not create a *prima facie* case for anticipation.

For at least this reason, Applicants respectfully assert that Merchant and Denio fail to teach all of the elements of claim 1 and the rejection thereof is improper and should be withdrawn. For at least the same reason, claims 2-9, dependent on claim 1, are also respectfully asserted to be allowable over the cited prior art.

Claims 10 and 13 recite, in part, "determining index values for the input data packets" and "means for determining index values for the input data packets", respectively. Thereafter, the index values are used by the fast filtering processor to rapidly find an indexed specific action of the specific actions. Neither Merchant nor Denio teaches or suggests determining and using index values to filter packets. The section of Denio that is apparently relied upon in the rejection is column 5, lines, 35-65, where heuristics used to include or exclude packets are discussed. However, no indexing is disclosed and no index values are used in any filtering decision.

The Office Action asserts that "Denio discloses using heuristics to forward only specific (indexed) data." If this rejection is maintained, it is respectfully requested that this assertion that the data is indexed (and how the index values for the input data packets

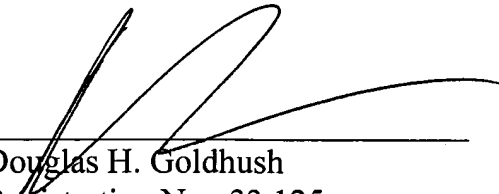
are determined) be explained. Indexing is not mentioned in the passage the Office Action cites, namely Col. 5, l. 35 – Col. 6, l. 43). Indeed, a search of Denio provides zero references to “index.” Accordingly, Applicants respectfully submit that the basis for the rejection is mistaken.

For at least this reason, Applicants respectfully assert that Merchant and Denio fail to teach all of the elements of claims 10 and 13 and the rejections thereof are improper and should be withdrawn. For at least the same reason, claims 11, 12, 14 and 15, dependent on claims 10 and 13, are also respectfully asserted to be allowable over the cited prior art.

It is further submitted that each of claims 1-15 recite subject matter which is neither disclosed nor suggested in the cited prior art. It is therefore respectfully requested that all of claims 1-15 be allowed, and this application passed to issue.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

  
\_\_\_\_\_  
Douglas H. Goldhush  
Registration No. 33,125

**Customer No. 32294**  
SQUIRE, SANDERS & DEMPSEY LLP  
14<sup>TH</sup> Floor  
8000 Towers Crescent Drive  
Tysons Corner, Virginia 22182-2700  
Telephone: 703-720-7800  
Fax: 703-720-7802

DHG/PCF:jf